What is claimed is:

1. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing two one-dimensional inverse discrete cosine transforming functions, each of the functions being controlled to operate on a matrix of coefficients in either of two different directions.

2. The method of claim 1 in which one of the directions is row order.

3. The method of claim 1 in which one of the directions is column order.

4. The method of claim 1 in which a sequencer determines which direction each function operates in for a given matrix.

5. The method of claim 1 in which an address generator generates an address for each coefficient in the matrix.

6. The method of claim 1 in which the functions are concurrently executed in the same direction on two different matrices of coefficients.

7. The method of claim 1 in which the functions are concurrently executed in the same direction, the functions

switching periodically and concurrently to the other direction.

8. A storage medium bearing a machine-readable program capable of causing a machine to:

execute two one-dimensional inverse discrete cosine transforming functions, each of the functions being controlled to operate on a matrix of coefficients in either of two different directions.

9. The medium of claim 8 in which one of the directions is row order.

10. The medium of claim 8 in which one of the directions is column order.

11. The medium of claim 8 in which a sequencer determines which direction each function operates in for a given matrix.

12. The medium of claim 8 in which an address generator generates an address for each coefficient in the matrix.

13. The medium of claim 8 in which the functions are concurrently executed in the same direction on two different matrices of coefficients.

14. The medium of claim 8 in which the functions are concurrently executed in the same direction, the functions

switching periodically and concurrently to the other direction.

15. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing a first one-dimensional inverse discrete cosine transforming function in a first direction on a first matrix of coefficients to produce a matrix of intermediate results; and

executing a second one-dimensional inverse discrete cosine transforming function in a second, different direction on the matrix of intermediate results concurrent with the first function executing in the second direction on a second matrix of coefficients.

16. The method of claim 15 in which the first direction is row order.

17. The method of claim 15 in which the first direction is column order.

18. The method of claim 15 in which the functions switch periodically and concurrently between the first and second directions.

19. A storage medium bearing a machine-readable program capable of causing a machine to:

execute a first one-dimensional inverse discrete cosine transforming function, where the first function executes in a first direction on a first matrix of coefficients, producing a matrix of intermediate results; and

execute a second one-dimensional inverse discrete cosine transforming function, where the second function executes in a second, different direction on the matrix of intermediate results concurrent with the first function executing in the second direction on a second matrix of coefficients.

20. The medium of claim 19 in which the first direction is row order.

21. The medium of claim 19 in which the first direction is column order.

22. The medium of claim 19 in which the functions switch periodically and concurrently between the first and second directions.

23. An apparatus implementing a two-dimensional inverse discrete cosine transform, comprising:

two one-dimensional inverse discrete cosine transform blocks;

a memory block;

a sequencer block, the sequencer block alternately being in one of two states, each state indicating the direction each

one-dimensional inverse discrete cosine transform block operates in; and

an address generator block.

24. The apparatus of claim 23 in which the address generator block is to generate addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer.

25. A computer system including a processor, comprising:

two one-dimensional inverse discrete cosine transform blocks;

a memory block;

a sequencer block, the sequencer block alternately being in one of two states, each state indicating the direction each one-dimensional inverse discrete cosine transform block operates in; and

an address generator block.

26. The system of claim 25 in which the address generator block is to generate addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer.

27. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing two one-dimensional inverse discrete cosine

transforming functions to operate on a sequence of matrices, some matrices being operated on first in row order, then in column order and some matrices being operated on first in column order, then in row order.

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